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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/029,848 | 12/31/2001 | Jae Hyung Lee | 049128-5034 | 5336 |

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| EXAMINER | |
|---|---|
| KUMAR, SRILAKSHMI K | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2629 | |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/029,848 | LEE ET AL. | |
| | Examiner | Art Unit | |
| | Srilakshmi K. Kumar | 2629 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *17 April 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-9,11,12 and 14-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,11,12,14-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

The following office action is in response to the Pre-Brief Conference Request. In compliance with the Conference Decision, the prosecution of the application is reopened, and the Finality of the previous office action has been withdrawn.

### *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. ***Claims 1-7, 11, 12, and 16-19*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishimura (U.S. Patent No. 2001/0002829) in view of Chiang (U.S. Patent No. 6,271,822).

With reference to **claims 1, 11, and 16**, Nishimura teaches a liquid crystal polarity inversion driver determining whether a polarity of a liquid crystal is inverted and inverting the polarity of the liquid crystal in accordance with the determined result (see paragraph 43-44); a first data polarity inversion driver (10-1) determining whether a first data transition has occurred

in a first set of data, and inverting the polarity of the first set of data in accordance with the determined result (see paragraph 49); a second data polarity inversion driver (10-2) determining whether a second data transition has occurred and inverting the polarity of the second set of data in accordance with the determined result (see paragraph 49). While the preferred embodiment of Nishimura teaches a four port data polarity inverter, Nishimura teaches in Fig. 8 where a two port polarity inverter can be used and further, each inverter has two ports.

Nishimura does not teach wherein the first set of data is odd numbered bits in an input data and the second set of data is even numbered bits in the input data. Chiang teaches in Fig. 2, item 221, a polarity inversion circuit. In col. 5, lines 21-47, Chiang teaches where the inversion circuit encompasses two sets of data, one where the data is odd numbered bits where they have a positive polarity, and the second being where the data is even numbered bits where they have a negative polarity.

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to allow that the data be divided into even and odd groups as taught by Chiang, to be used in a system similar to that which is taught by Nishimura, which allows for 2-port data polarity inversion. By allowing such a combination a large high-resolution liquid crystal display with a reduction in power consumption would result (see Chiang col. 4, lines 19-24).

With reference to **claims 2, 3, 12, and 17**, Nishimura teaches that the first data polarity inversion driver includes, a first data transition part (11) determining whether the first data transition has occurred in the first/odd data and outputting a first signal (inv1) (see paragraph 53); a first data polarity inversion signal summer (12) counting the number of first signal that a data polarity has changed according to the first data transition and determining whether an output

level is high or low (see paragraph 53); and a first data polarity inversion signal output part (15) receiving the first signal and the determined output level from the first data transition part and the first data polarity inversion signal summer and outputting an inverting signal (dd1-24) for inverting output data (paragraph 53, Fig. 4). With further reference to **claims 3 and 17**, Nishimura teaches that the components of data polarity inversion judgment units (10-1 through 10-4) have the same construction, therefore the construction of the second/even data polarity inversion driver (10-2) has the same construction to that which is described with reference to the first data polarity inversion driver (10-1) (see paragraph 52).

With reference to **claims 4, 5, and 18**, Nishimura teaches that the first and second data transition part includes first (13) and second (14) flip-flops and an exclusive logical sum gate (23) comparing current data with previous data to determine whether the first data transition has occurred in accordance with the compared result (see paragraph 53).

With reference to **claims 6, 7, and 19**, Nishimura teaches that the first and second data inversion signal summer includes an a first and second adder for adding the number of data with a data transition from the first and second data transition part; and a majority detector (22) determining whether the added number of the data is higher than a first and second reference value (see paragraph 53-57).

4. **Claims 8, 9, and 20** are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishimura in view of Chiang as applied to **claims *1-7, 11, 12, and 16-19*** above, and further in view of Applicant's admittance of prior art.

**Claims 8, 9, and 20** are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishimura in view of Chiang as applied to **claims *1-7, 11, 12, and 16-19*** above, and further in view of Applicant's admittance of prior art.

Nishimura and Chiang teach all that is required as explained above with reference to **claims 1, 11, and 16**, however fails to teach that the data polarity inversion signal output part includes a multiplexer receiving the signal from the summer to invert the output data. However, there is no disclosure relating to the applicant's invention of the usage of a summer and outputting inverted data as explained above.

Applicant's admitted prior art teaches as first data polarity inversion signal output part which includes a multiplexer (48, 50) receiving a first polarity inversion signal from the first data polarity inversion signal summer (32) to invert the output data (see paragraph 23).

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to allow the output part to consist of a multiplexer, as disclosed by the applicant's admittance of prior art, in a system composed similar to that which is taught by Nishimura and Chiang as explained above to thereby provide a liquid crystal display which outputs inverted data to be applied to the liquid crystal panel in order to reduce the amount of change of data output which reduces power consumption and noise generated.

5. **Claims 14 and 15** are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishimura in view of Chiang as applied to **claims *1-7, 11, 12, and 16-19*** above, and further in view of Gooding et al. (U.S. Patent No. 4,580,265).

Nishimura and Chiang teach all that is required as explained above with reference to **claims 1, 11, and 16** as explained above, however fail to teach that the total number of bits is 18 and the first and second data bits it 9 as recited in the claim.

Gooding et al. teaches an integrated circuit (10) connected to a second circuit (12) wherein the first circuit (10) receives the even and odd bytes of data to be transmitted to the second circuit (12), wherein the even and odd bytes of data each comprise nine binary bits. Thereby the total number of the input data bit is 18.

Therefore it would have been obvious to one having ordinary skill in the art to allow for the usage even and odd data bits being inputted into a IC as taught by Gooding, to be used in a system similar to that which is taught by Nishimura and Chiang as explained above in order to reduce the transmission of erroneous data and thereby reduce the effects of EMI on the display (see Gooding et al. column 2, lines 13-26).

***Response to Arguments***

6. Applicant's arguments filed April 17, 2007 have been fully considered but they are not persuasive.

Applicant argues where the prior art of Nishimura does not teach a two port polarity inverter, but teaches a four port polarity inverter, and thus can not meet the limitations set forth in the instant application. Examiner, respectfully, disagrees. The claim limitation does not limit the polarity inverter to only two ports. Further, Nishimura teaches in Fig. 8 where a two port polarity inverter can be used and further, each inverter has two ports.

Applicants argues were Nishimura fails to teach or suggest a first data polarity inversion driver determining whether a first data transition has occurred in the odd numbered bits of data

and a second data polarity inversion driver determining whether a second data transition has occurred in the even numbered bits of data. Nishimura teaches a first data polarity inversion driver (10-1) determining whether a first data transition has occurred in a first set of data, and inverting the polarity of the first set of data in accordance with the determined result (see paragraph 49); a second data polarity inversion driver (10-2) determining whether a second data transition has occurred and inverting the polarity of the second set of data in accordance with the determined result (see paragraph 49). Examiner agrees that Nishimura fails to teach where wherein the first set of data is odd numbered bits in an input data and the second set of data is even numbered bits in the input data. The prior art of Chiang is added to teach a polarity inversion circuit which encompasses two sets of data, one of the odd numbered bits, and the other of even numbered bits in Fig. 2, item 221, and col. 5, lines 21-47. The prior art of Chiang is added to teach two different data sets. With respect to applicant's arguments of where the prior art of Nishimura teaches away from Chiang, examiner, respectfully disagrees. The combination of Nishimura and Chiang is proper as the prior art of Chiang enables using odd and even groups in the polarity inverter, and further, enables a large high resolution liquid crystal display with a reduction in power consumption (Chiang col. 4, lines 19-24). Therefore, the prior art teaches the limitations set forth in the instant application, thus the rejection is maintained and made FINAL.

***Conclusion***

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Srilakshmi K. Kumar whose telephone number is 571 272 7769. The examiner can normally be reached on 9:00 am to 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Lefkowitz can be reached on 571 272 3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Srilakshmi K Kumar
Examiner
Art Unit 2629

SKK
July 4, 2007

SUMATI LEFKOWITZ
SUPERVISORY PATENT EXAMINER